

34. (New) The process of claim 28, wherein the silicon oxide layer is deposited to a thickness of about 1000-3000 Angstroms and can be adjusted according to design rules.

35. (New) The process of claim 28, wherein the step of forming the cap layer includes depositing a silicon oxide layer using a chemical vapor deposition method with tetra-ethyl-ortho-silicate (TEOS) as the main reactive agent.

36. (New) The process of claim 28, wherein the silicon oxide layer is deposited to a thickness of about 1000-3000 Angstroms and can be adjusted according to design rules.

37. (New) The process of claim 28, wherein the step of forming the cap layer includes depositing a silicon nitride layer using a chemical vapor deposition method with silane (SiH_4) as the main reactive agent.

38. (New) The process of claim 28, wherein the silicon nitride layer is deposited to a thickness of about 100-3000 Angstroms and can be adjusted according to design rules.

39. (New) The process of claim 28, wherein the step of forming the cap layer includes depositing a silicon nitride layer using a chemical vapor deposition method with silicon dichlorohydride (SiH_2Cl_2) as the main reactive agent.

40. (New) The process of claim 28, wherein the silicon nitride layer is deposited to a thickness of about 100-3000 Angstroms and can be adjusted according to design rules.

41. (New) The process of claim 28, wherein the step of forming the cap layer includes depositing silicon dioxide.

42. (New) The process of claim 28, wherein the step of forming the cap layer includes depositing phosphosilicate glass (PSG).

43. (New) The process of claim 28, wherein the step of forming the cap layer includes depositing silicon-rich oxide (SRO).

44. (New) A process of forming a conductive interconnect, the process comprising the steps of:

- providing a semiconductor substrate having a conductive layer thereon;
- forming a dielectric layer over the substrate and the conductive layer;
- polishing the surface of the dielectric layer to form a substantially planar surface; and
- forming a dielectric cap layer over the dielectric layer.

Sheet 1 of 1